FIG. 1

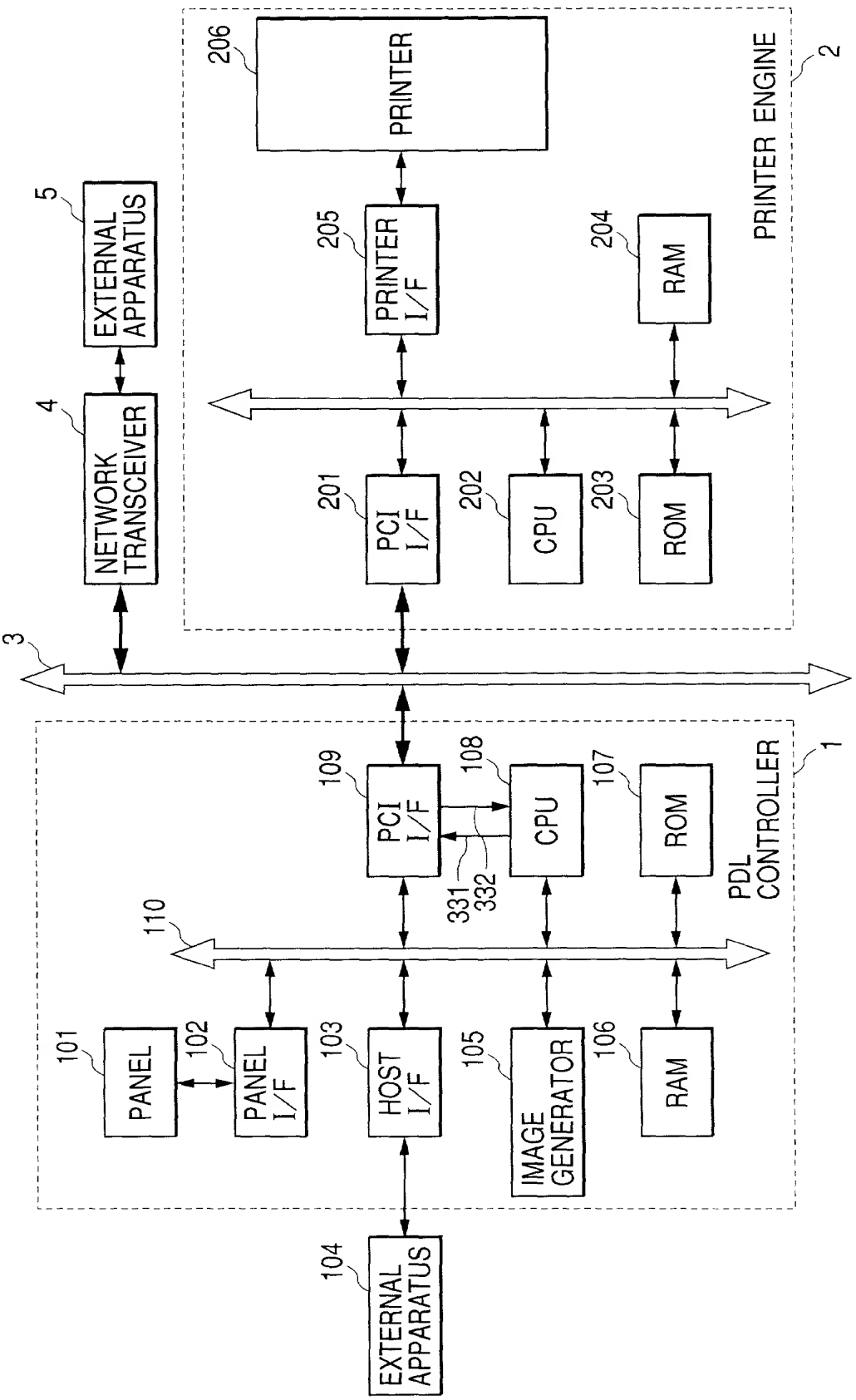

PDL CONTROLLER
1
PRINTER ENGINE
2
3
4
5
101
PANEL
102
PANEL I/F
103
HOST I/F
104
EXTERNAL APPARATUS
105
IMAGE GENERATOR
106
RAM
107
ROM
108
CPU
109
PCI I/F
110
331
332
201
PCI I/F
202
CPU
203
ROM
204
RAM
205
PRINTER I/F
206
PRINTER
NETWORK TRANSCEIVER
EXTERNAL APPARATUS

FIG. 2

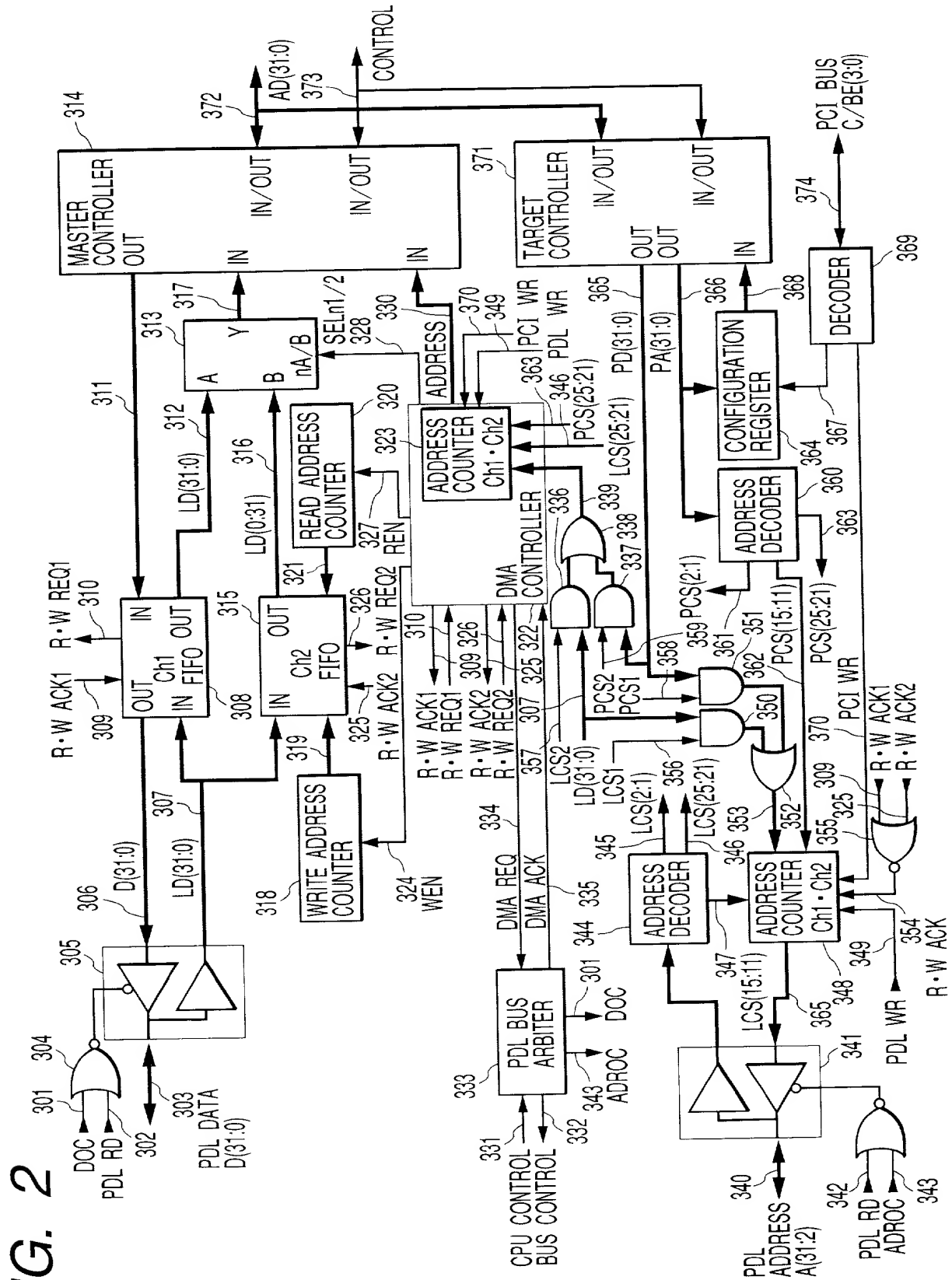
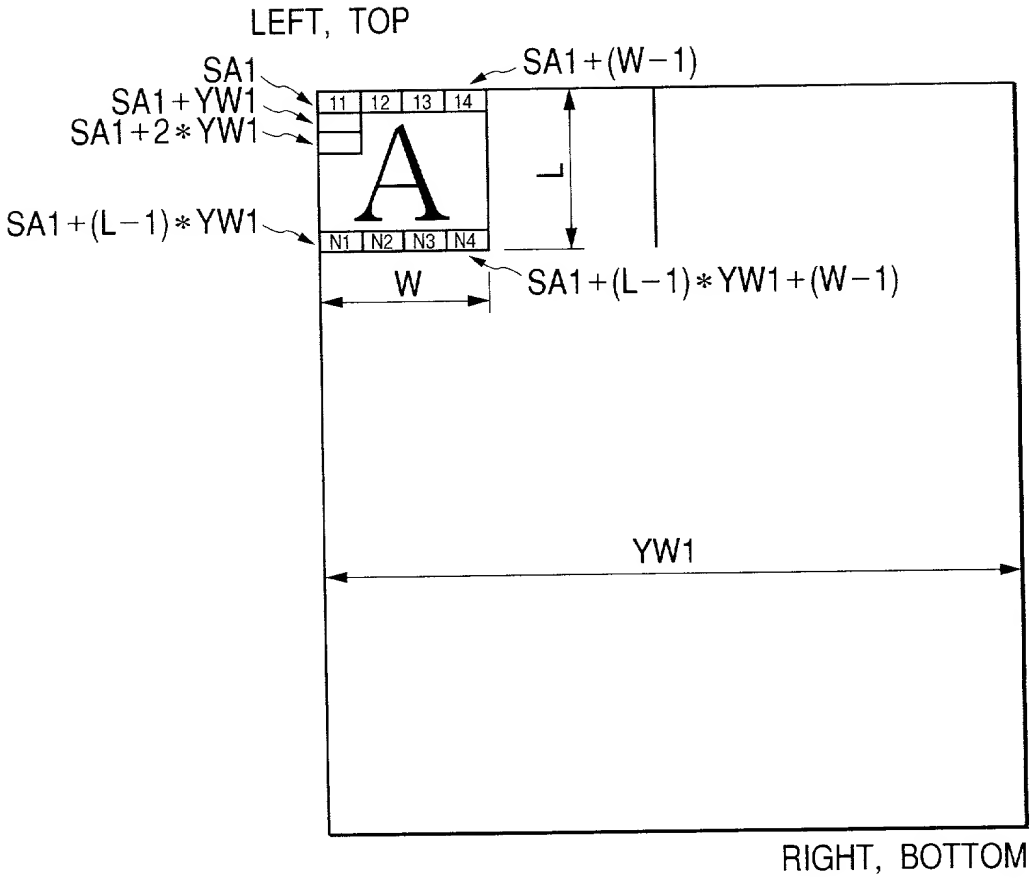
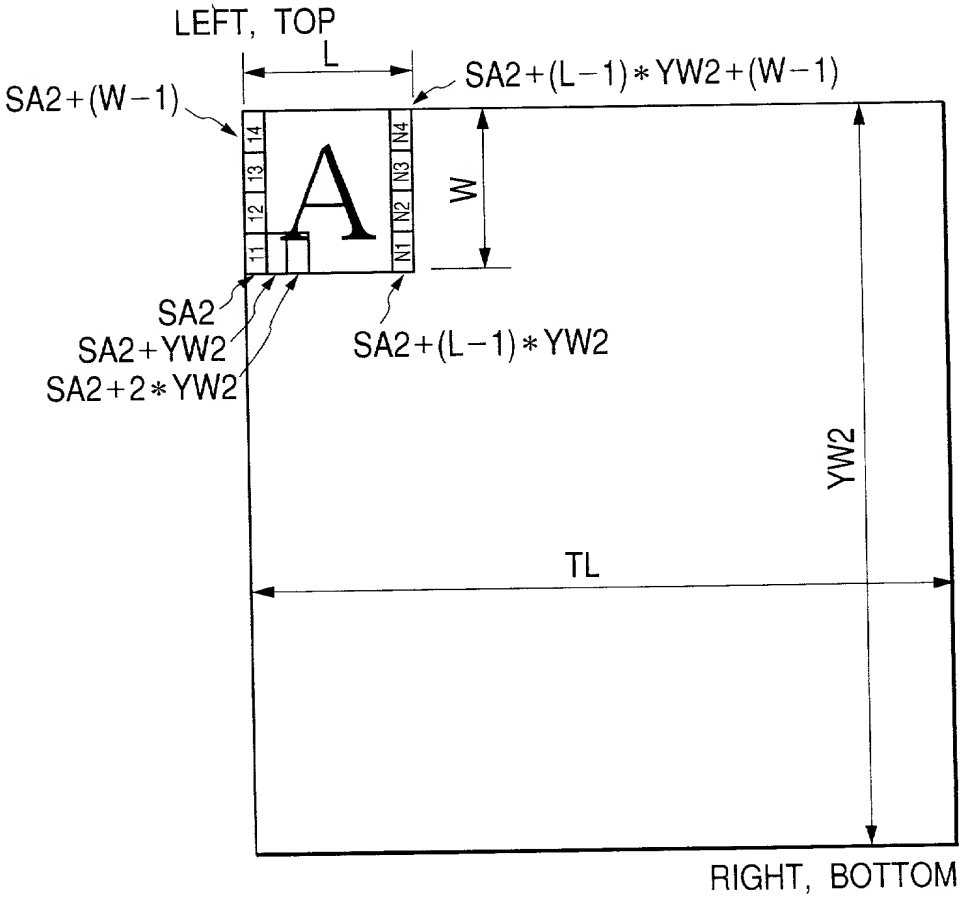

MASTER CONTROLLER
TARGET CONTROLLER
DMA CONTROLLER
PDL BUS ARBITER
Ch1 FIFO
Ch2 FIFO
READ ADDRESS COUNTER
WRITE ADDRESS COUNTER
ADDRESS COUNTER Ch1 · Ch2
ADDRESS DECODER
CONFIGURATION REGISTER
DECODER
AD(31:0)
CONTROL
PCI BUS C/BE(3:0)
LD(31:0)
LD(0:31)
PD(31:0)
PA(31:0)
PCS(25:21)
PCS(15:11)
PCS(2:1)
LCS(25:21)
LCS(15:11)
LCS(2:1)
LCS1
LCS2
LD(31:0)
PCI WR
PDL WR
R · W ACK1
R · W REQ1
R · W ACK2
R · W REQ2
REN
WEN
DMA REQ
DMA ACK
D(31:0)
PDL DATA D(31:0)
DOC
PDL RD
ADROC
CPU CONTROL BUS CONTROL
PDL ADDRESS A(31:2)
R · W ACK

FIG. 3



PRINT DATA IN PDL BOARD MEM

FIG. 4



PRINT DATA IN ENGINE MEM

FIG. 5

CONDITION 1: ((LCS11='1' OR PCS11='1') AND (PCIWR='1' OR PDLWR='1')) SA1<=DT;
CONDITION 2: ((LCS12='1' OR PCS12='1') AND (PCIWR='1' OR PDLWR='1')) YW1<=DT;
CONDITION 3: ((LCS13='1' OR PCS13='1') AND (PCIWR='1' OR PDLWR='1')) W<=DT;
CONDITION 4: ((LCS14='1' OR PCS14='1') AND (PCIWR='1' OR PDLWR='1')) L<=DT;
CONDITION 5: ((LCS15='1' OR PCS15='1') AND (PCIWR='1' OR PDLWR='1')) ST<='1';

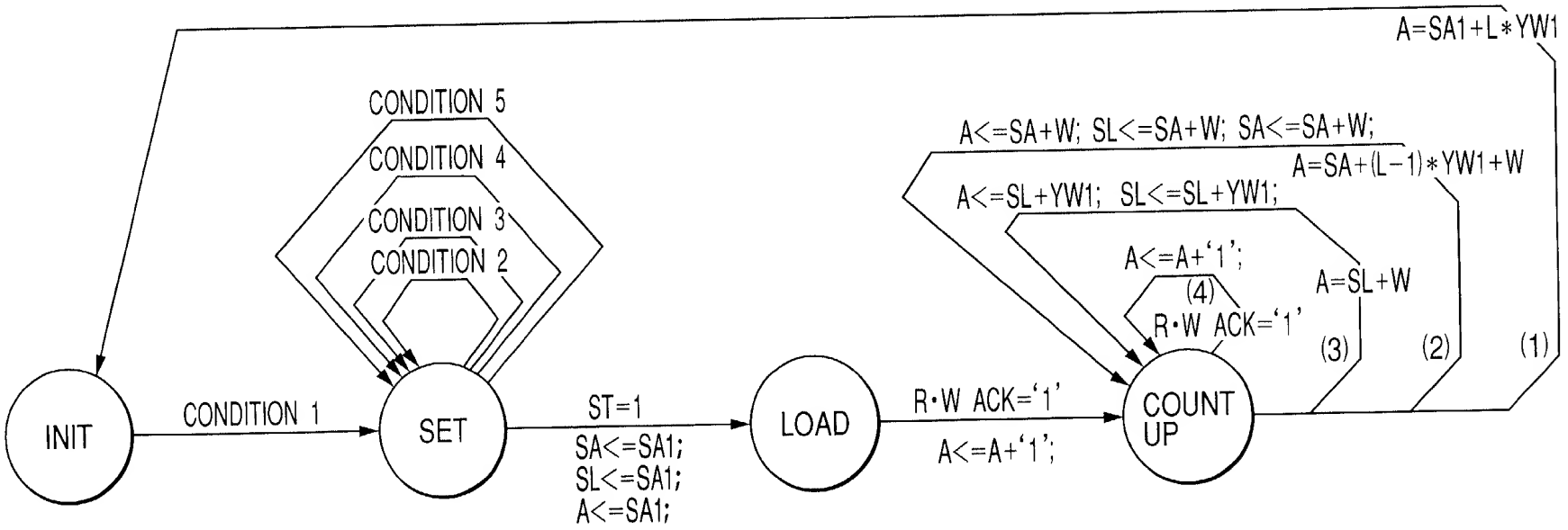


FIG. 6

CONDITION 1: ((LCS21='1' OR PCS21='1') AND (PCIWR='1' OR PDLWR='1')) SA2<=DT;
CONDITION 1: ((LCS22='1' OR PCS22='1') AND (PCIWR='1' OR PDLWR='1')) YW2<=DT;
CONDITION 1: ((LCS23='1' OR PCS23='1') AND (PCIWR='1' OR PDLWR='1')) W<=DT;
CONDITION 1: ((LCS24='1' OR PCS24='1') AND (PCIWR='1' OR PDLWR='1')) L<=DT;
CONDITION 1: ((LCS25='1' OR PCS25='1') AND (PCIWR='1' OR PDLWR='1')) TL<=DT; ST<='1';

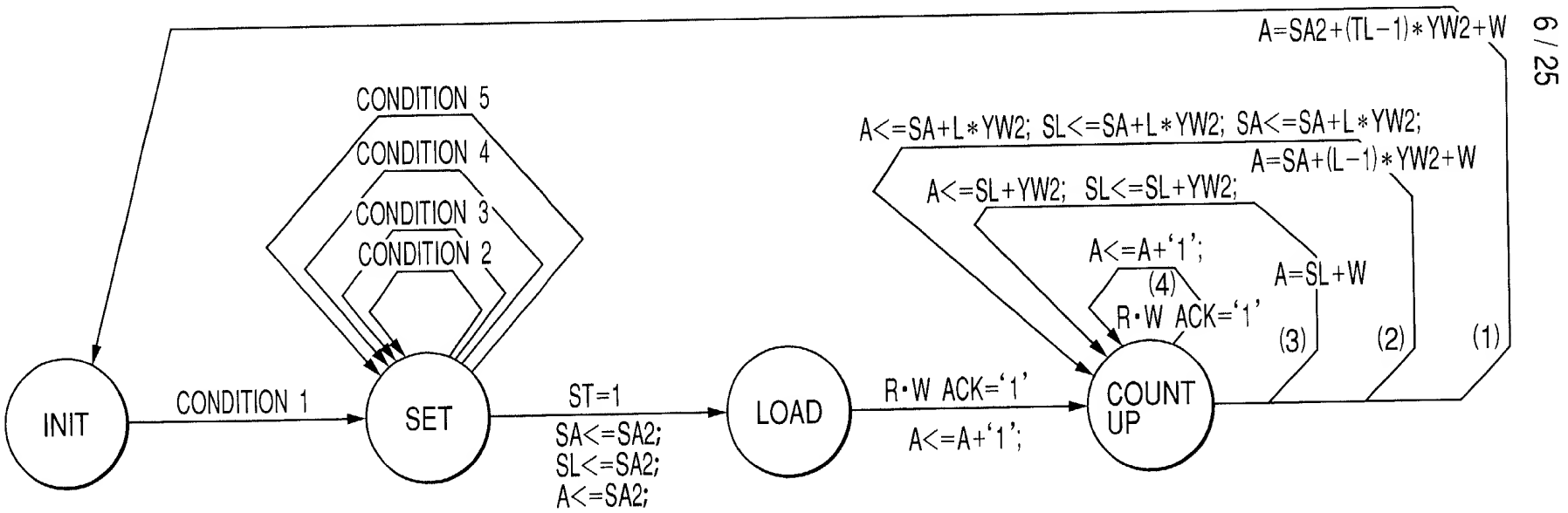
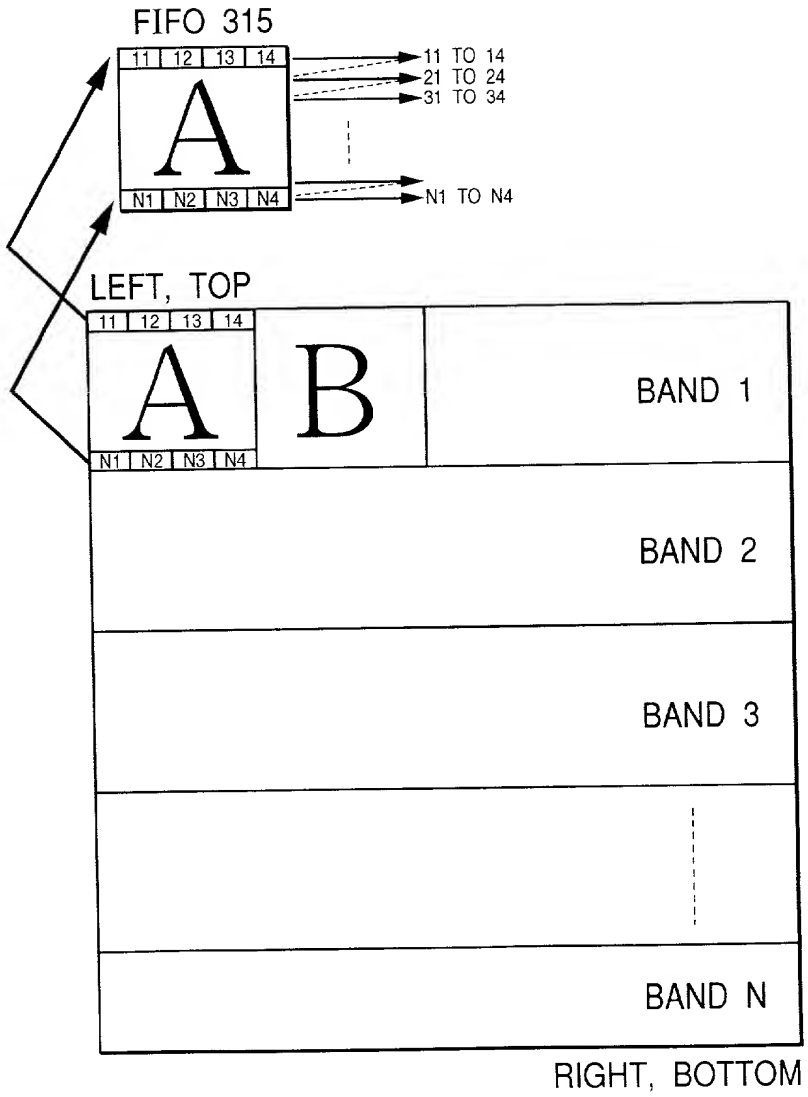
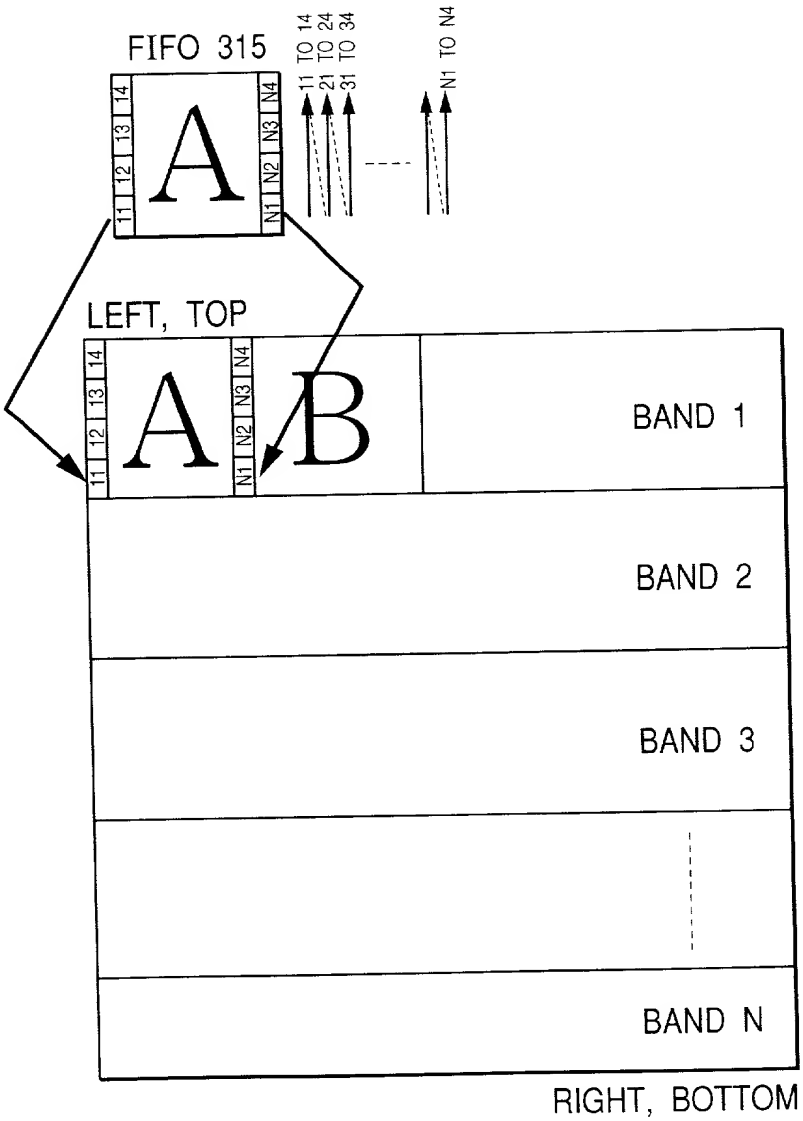


FIG. 7



PRINT DATA IN PDL BOARD MEM

FIG. 8



PRINT DATA IN ENGINE MEM

FIG. 9

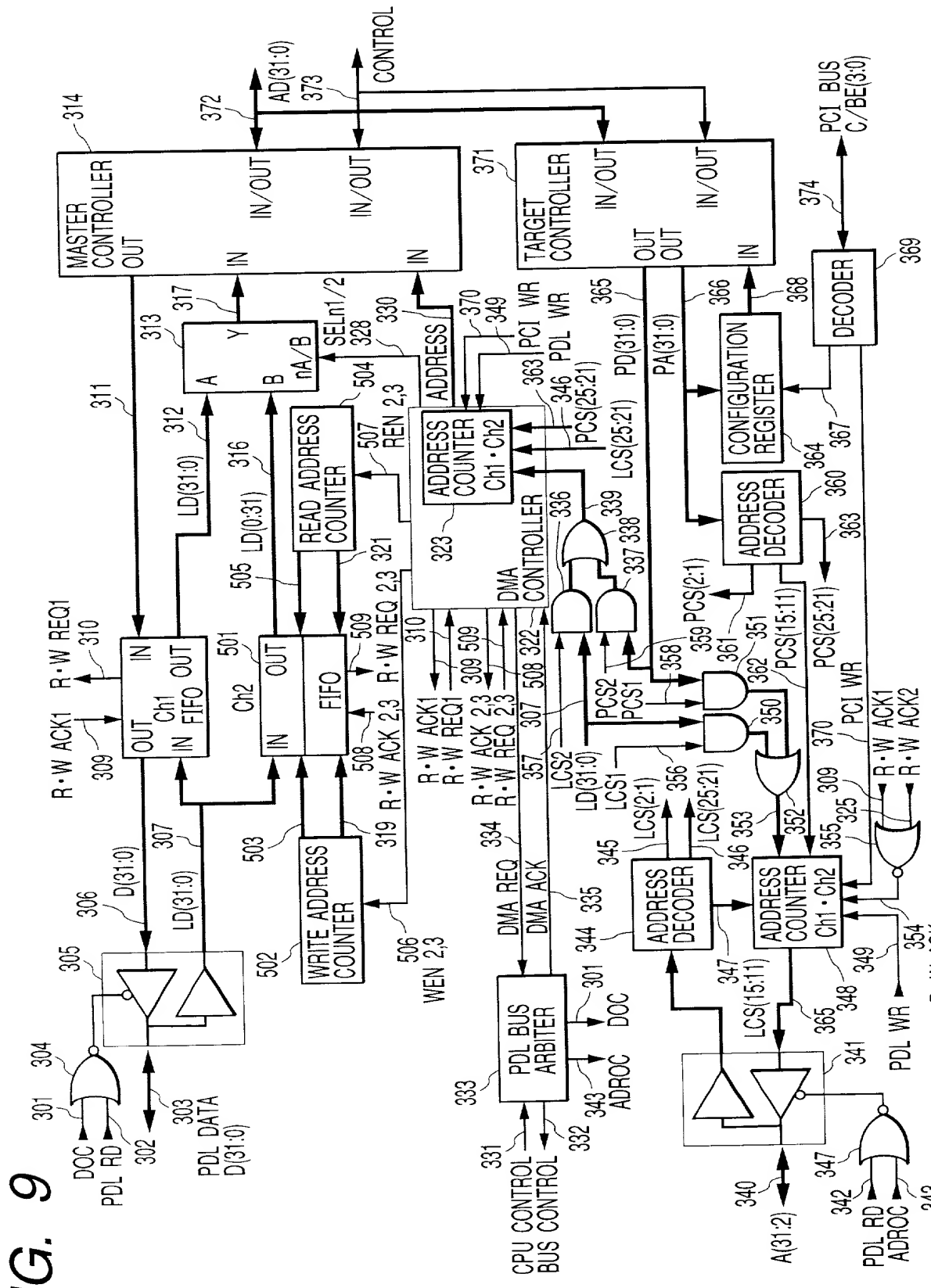
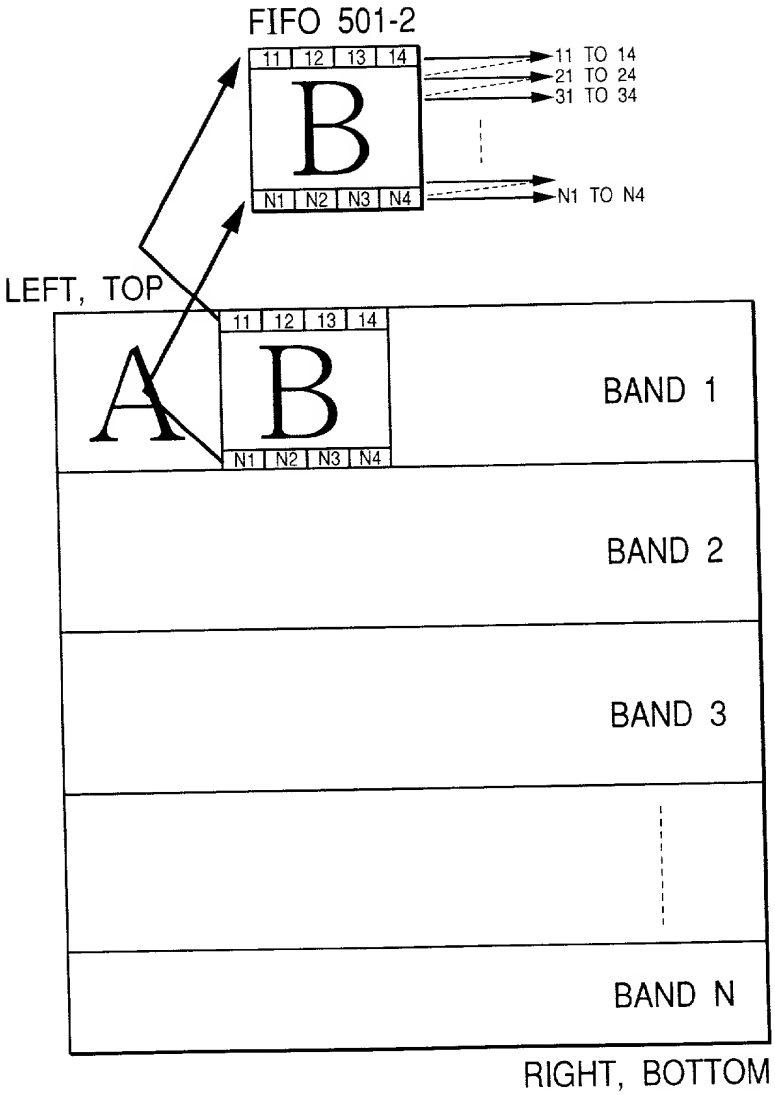

MASTER CONTROLLER
TARGET CONTROLLER
AD(31:0)
CONTROL
PCI BUS C/BE(3:0)
DECODER
CONFIGURATION REGISTER
ADDRESS DECODER
ADDRESS COUNTER Ch1・Ch2
READ ADDRESS COUNTER
WRITE ADDRESS COUNTER
FIFO
DMA CONTROLLER
PDL BUS ARBITER
DOC
PDL RD
PDL DATA D(31:0)
CPU CONTROL BUS CONTROL
A(31:2)
PDL WR
ADROC
R・W REQ1
R・W ACK1
R・W ACK2
R・W ACK
PCI WR
PDL WR
LD(31:0)
LD(0:31)
PA(31:0)
PD(31:0)
PCS(25:21)
PCS(15:11)
PCS(2:1)
LCS(25:21)
LCS(15:11)
LCS(2:1)
WEN 2,3
REN 2,3
DMA REQ
DMA ACK

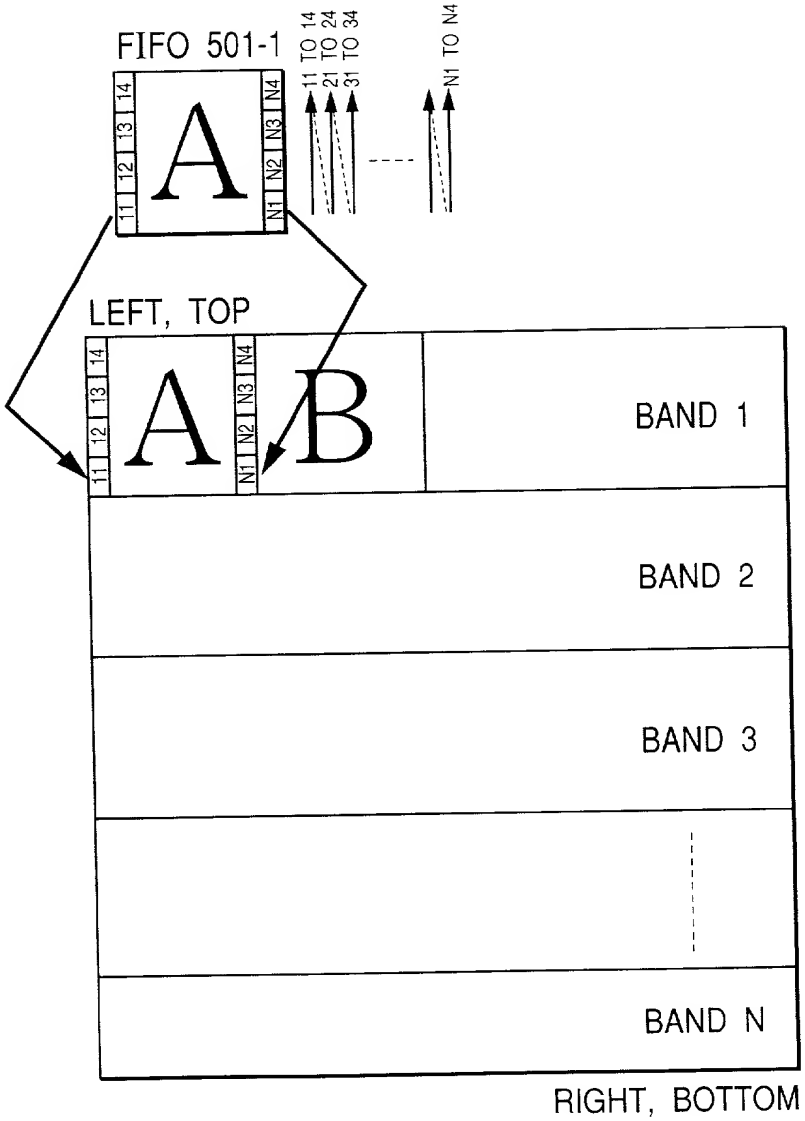
FIG. 10



PRINT DATA IN PDL BOARD MEM

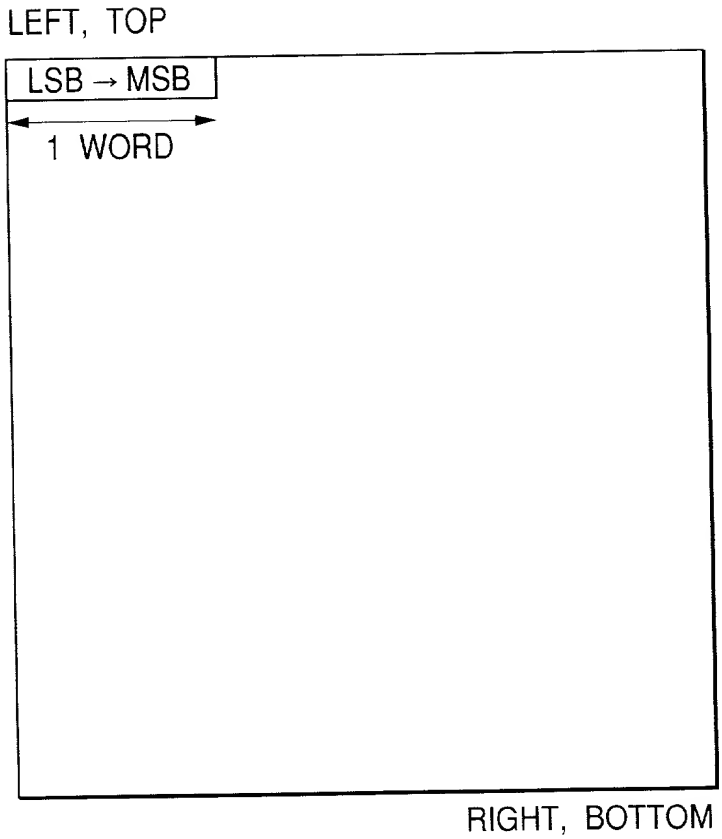
EP 0 954 165 A2

FIG. 11



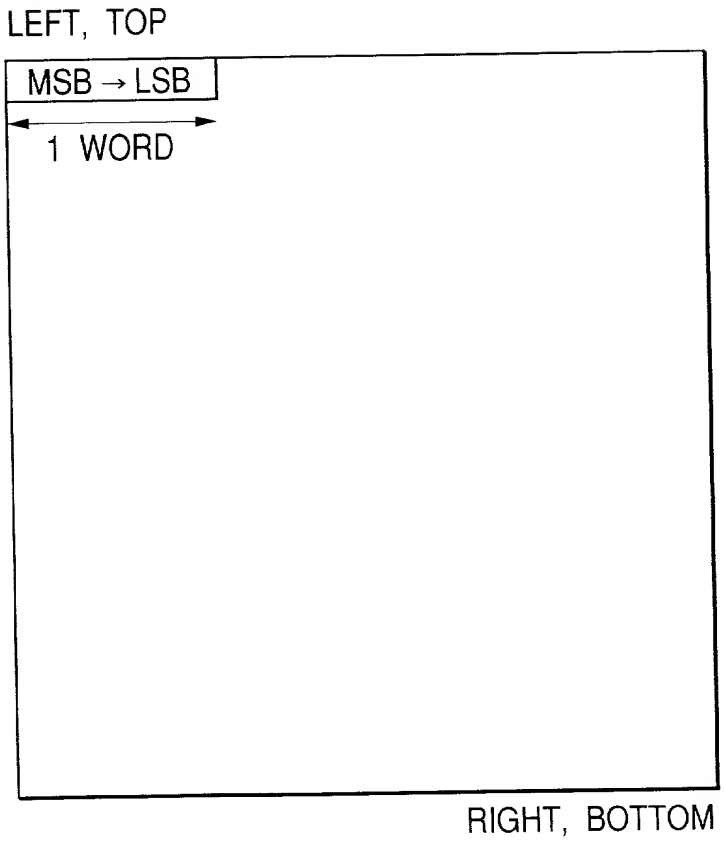
PRINT DATA IN ENGINE MEM

FIG. 12



PRINT DATA IN PDL BOARD MEM

FIG. 13



PRINT DATA IN ENGINE MEM

FIG. 14

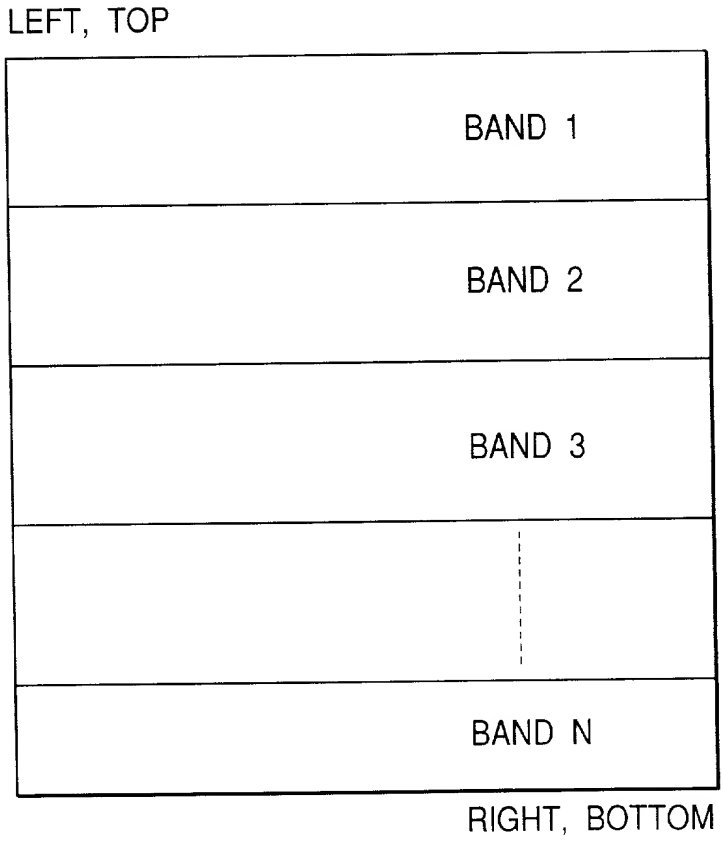

LEFT, TOP
BAND 1
BAND 2
BAND 3
BAND N
RIGHT, BOTTOM
PRINT DATA IN PDL BOARD MEM

FIG. 15

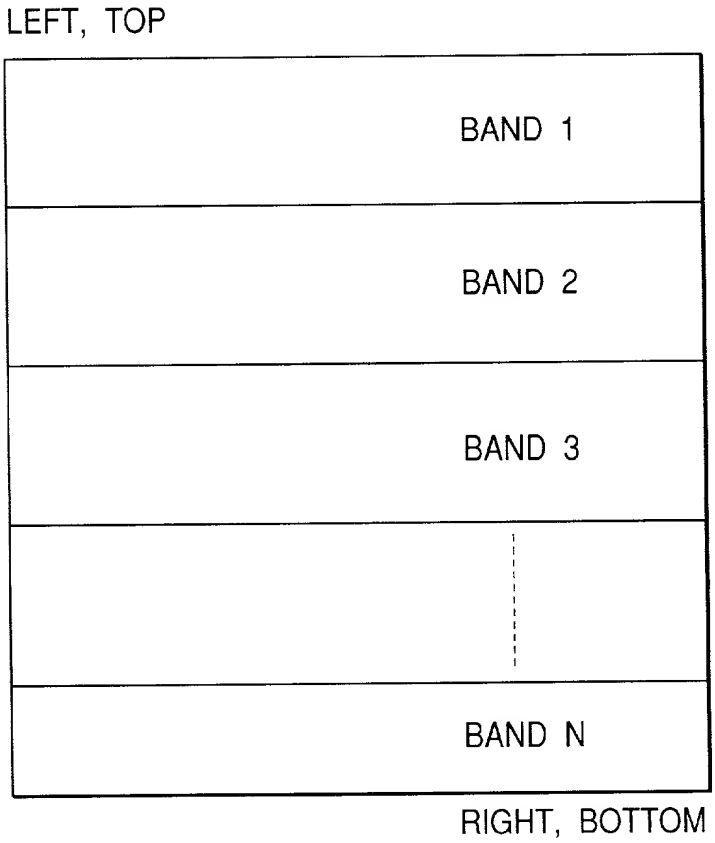

LEFT, TOP
BAND 1
BAND 2
BAND 3
BAND N
RIGHT, BOTTOM
PRINT DATA IN ENGINE MEM

FIG. 16

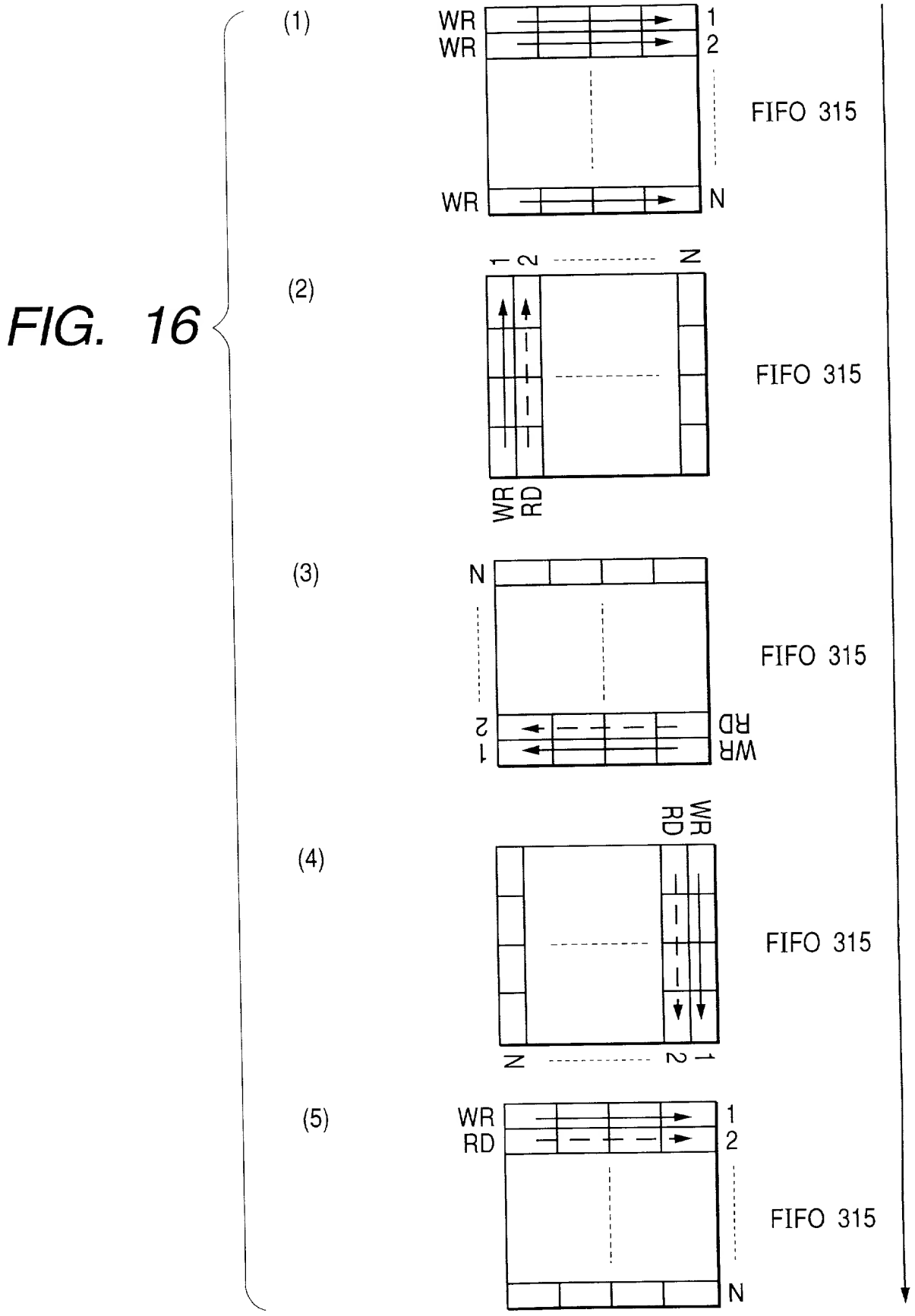


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FIG. 17

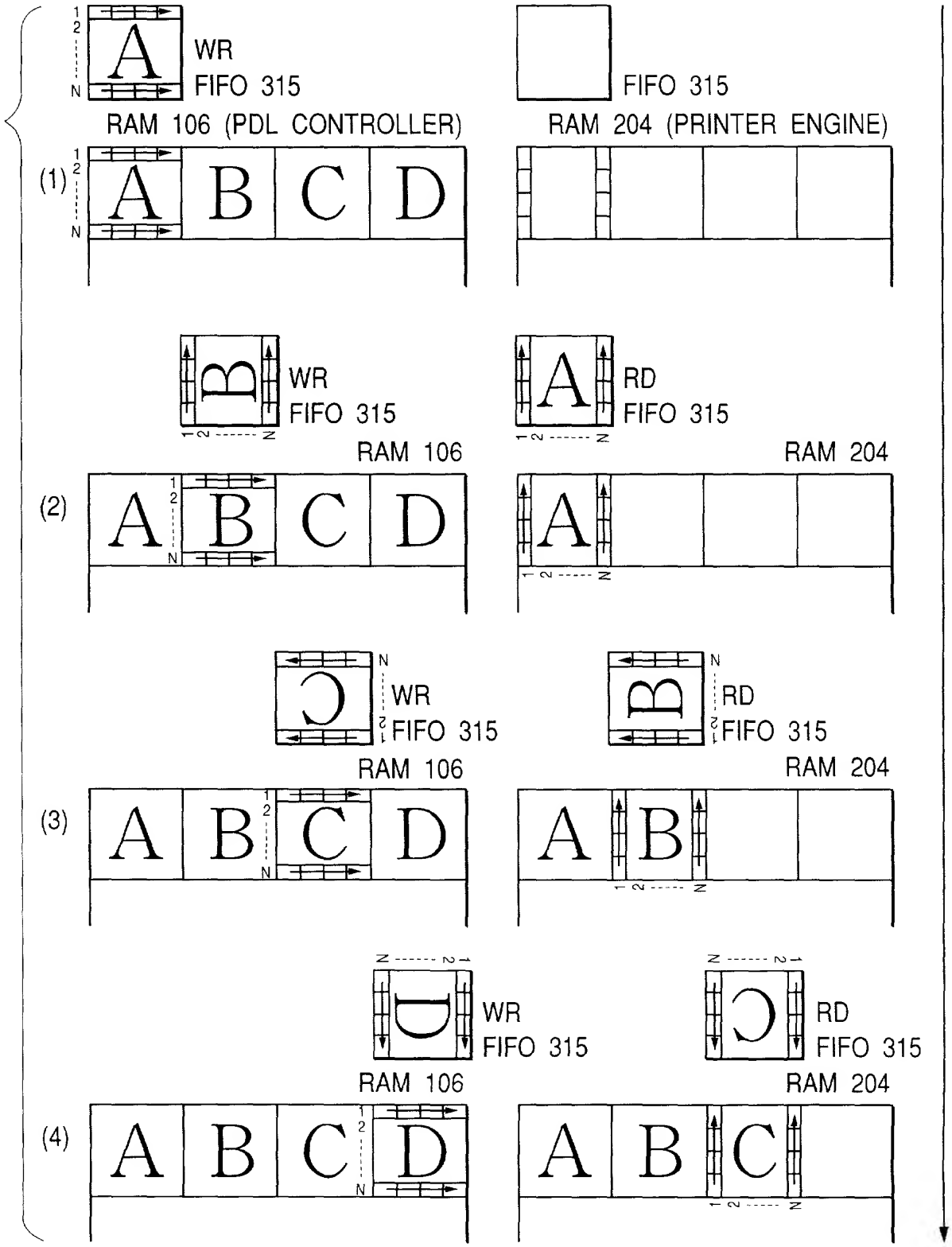
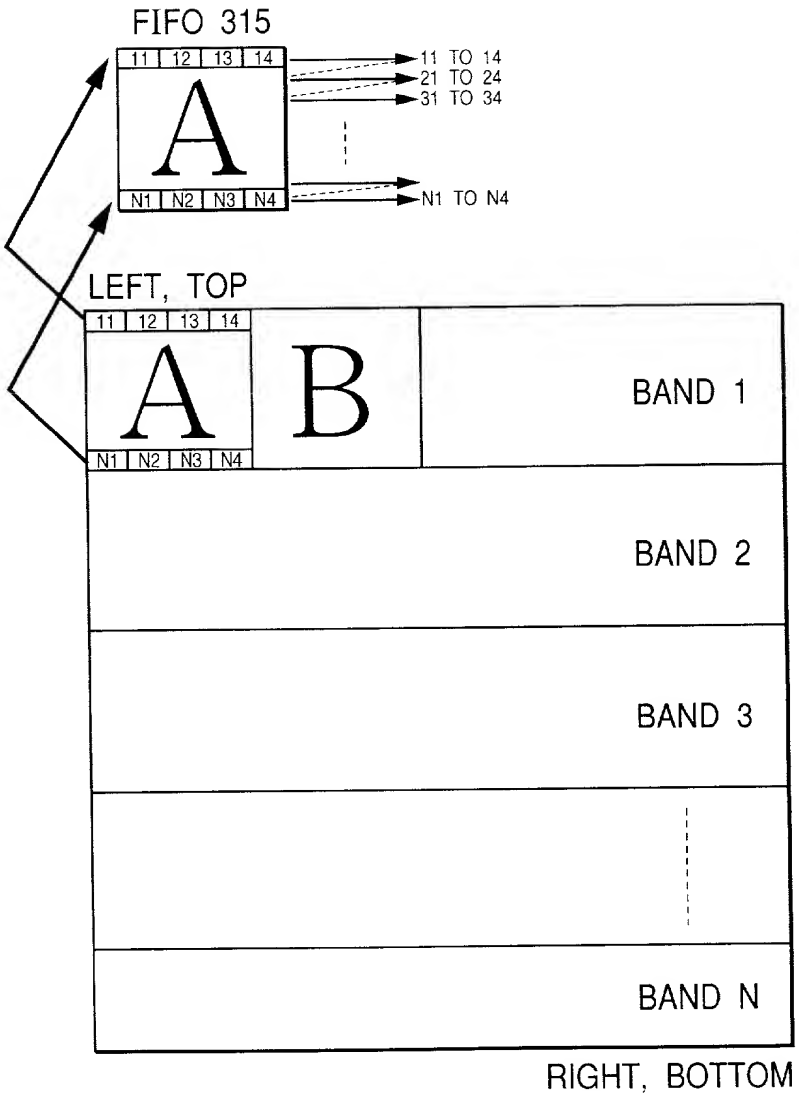
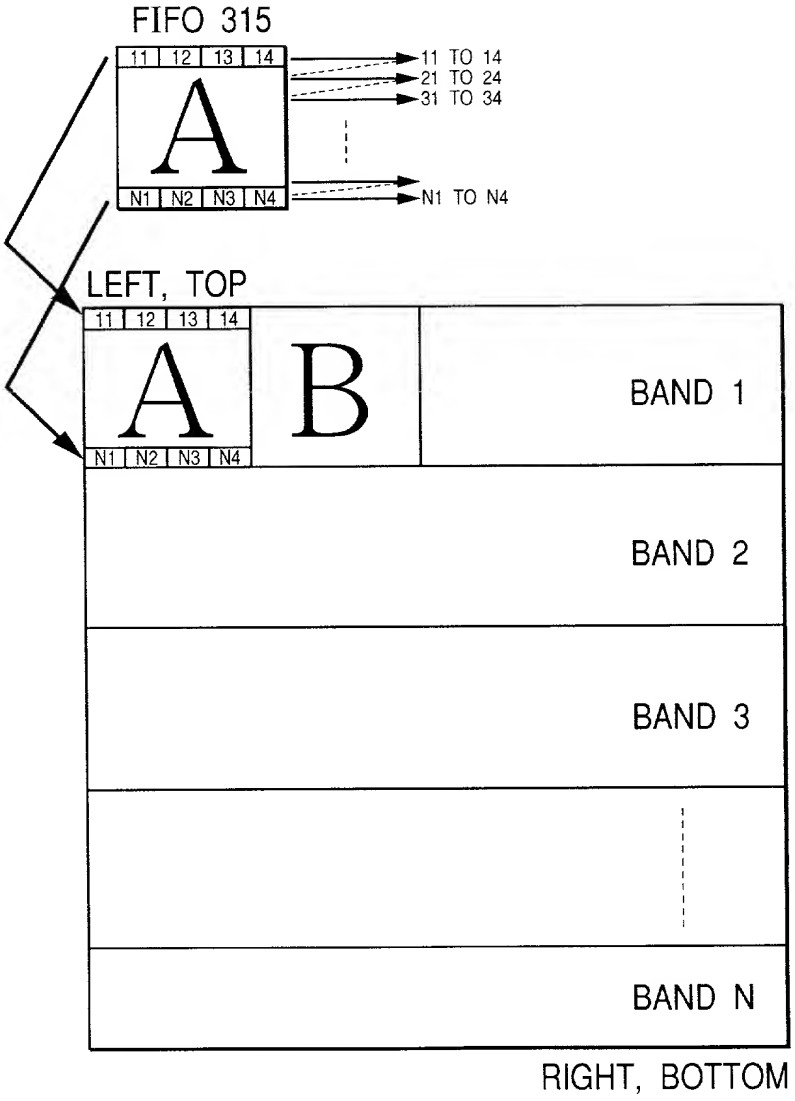

WR
FIFO 315
FIFO 315
RAM 106 (PDL CONTROLLER)
RAM 204 (PRINTER ENGINE)
(1)
RD
(2)
(3)
(4)
RAM 106
RAM 204

FIG. 18



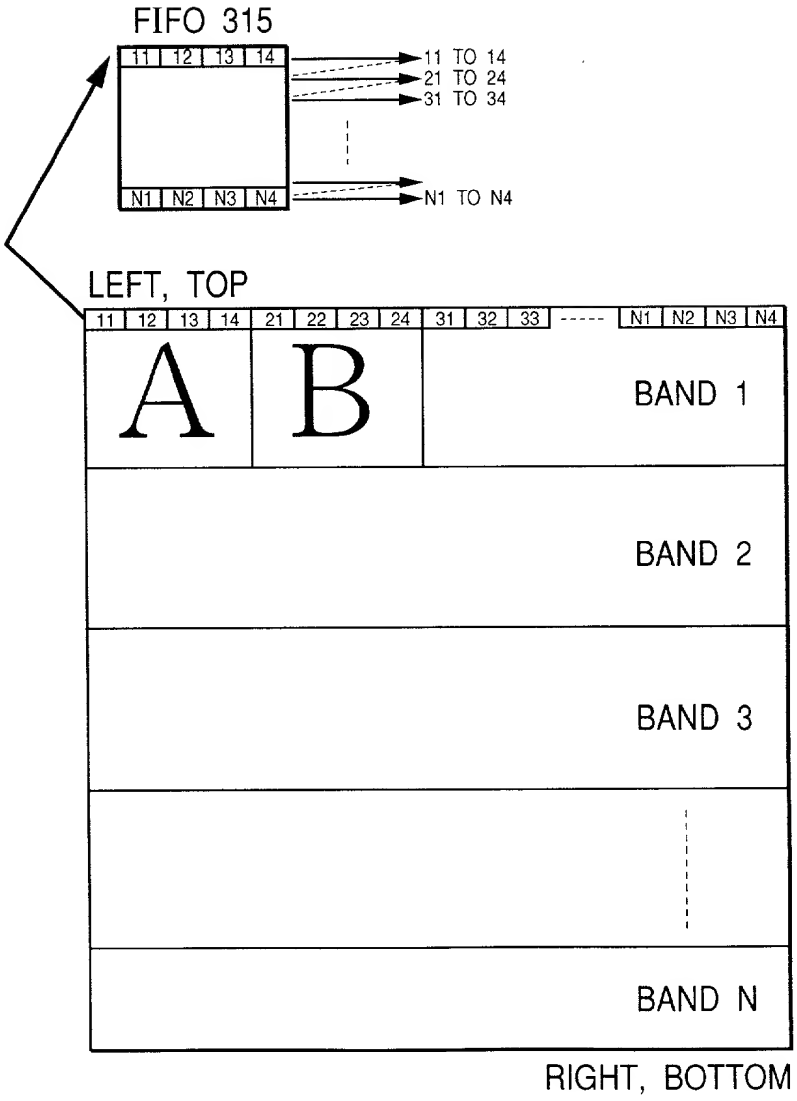
PRINT DATA IN PDL BOARD MEM

FIG. 19



PRINT DATA IN ENGINE MEM

FIG. 20



PRINT DATA IN PDL BOARD MEM

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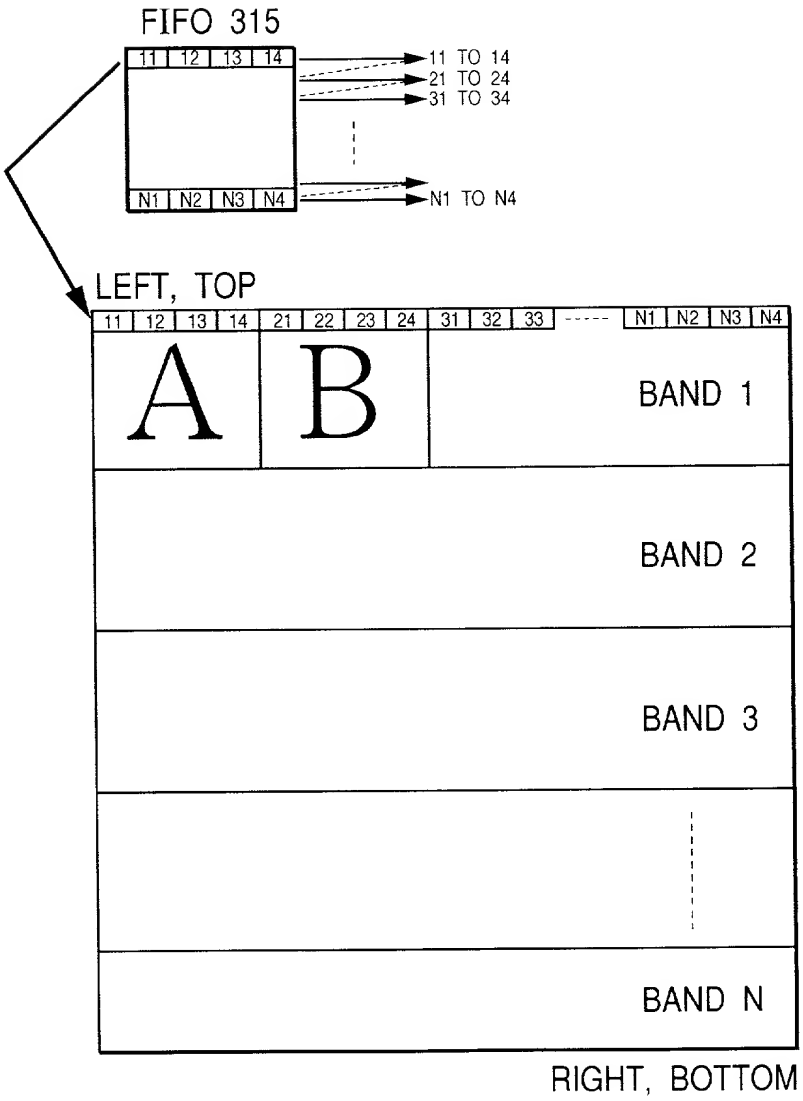
FIG. 21



PRINT DATA IN ENGINE MEM

FIG. 22

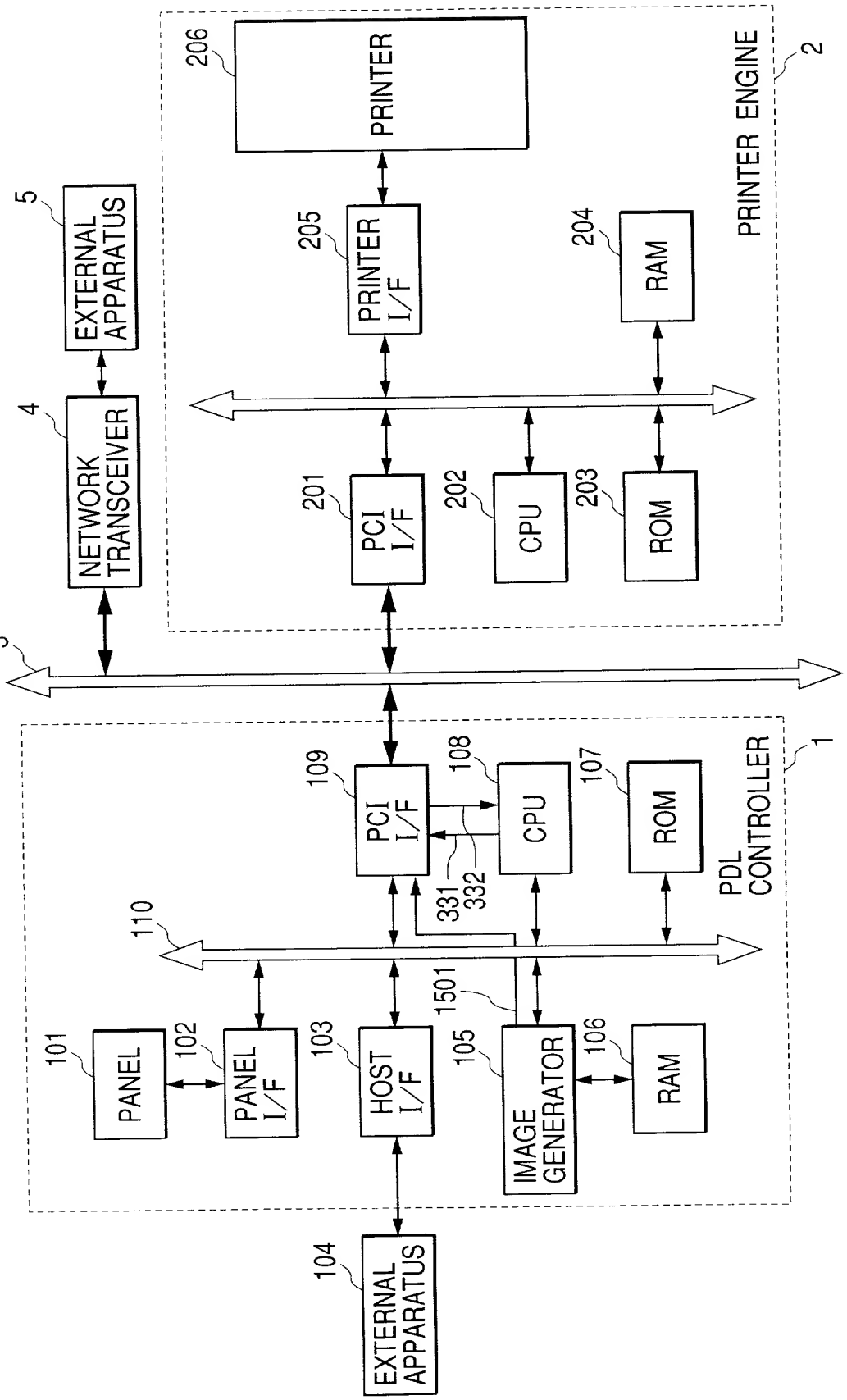

PDL CONTROLLER
1
PRINTER ENGINE
2
3
4
NETWORK TRANSCEIVER
5
EXTERNAL APPARATUS
PANEL
101
102
PANEL I/F
103
HOST I/F
104
EXTERNAL APPARATUS
105
IMAGE GENERATOR
106
RAM
107
ROM
108
CPU
109
PCI I/F
110
331
332
1501
201
PCI I/F
202
CPU
203
ROM
204
RAM
205
PRINTER I/F
206
PRINTER

FIG. 23

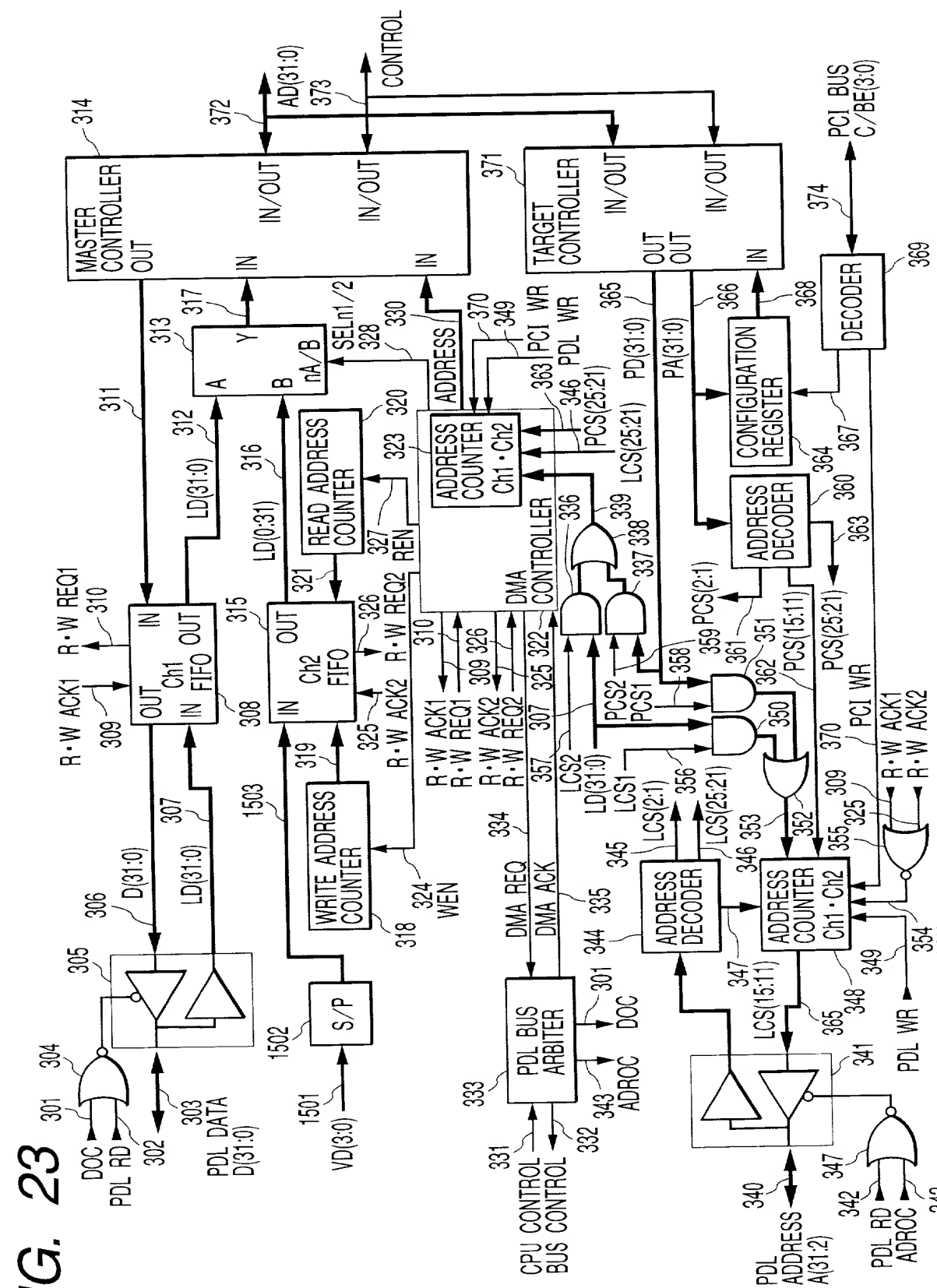

MASTER CONTROLLER
TARGET CONTROLLER
AD(31:0)
CONTROL
PCI BUS C/BE(3:0)
DECODER
CONFIGURATION REGISTER
ADDRESS DECODER
ADDRESS COUNTER Ch1・Ch2
READ ADDRESS COUNTER
WRITE ADDRESS COUNTER
Ch1 FIFO
Ch2 FIFO
DMA CONTROLLER
PDL BUS ARBITER
S/P
ADDRESS
LD(31:0)
LD(0:31)
PD(31:0)
PA(31:0)
LCS(25:21)
PCS(25:21)
LCS(15:11)
PCS(15:11)
LCS(2:1)
PCS(2:1)
LCS1
LCS2
PCS1
PCS2
PCI WR
PDL WR
REN
WEN
DMA REQ
DMA ACK
R・W REQ1
R・W ACK1
R・W REQ2
R・W ACK2
R・W ACK
D(31:0)
PDL DATA D(31:0)
DOC
PDL RD
ADROC
VD(3:0)
CPU CONTROL BUS CONTROL
PDL ADDRESS A(31:2)

FIG. 24

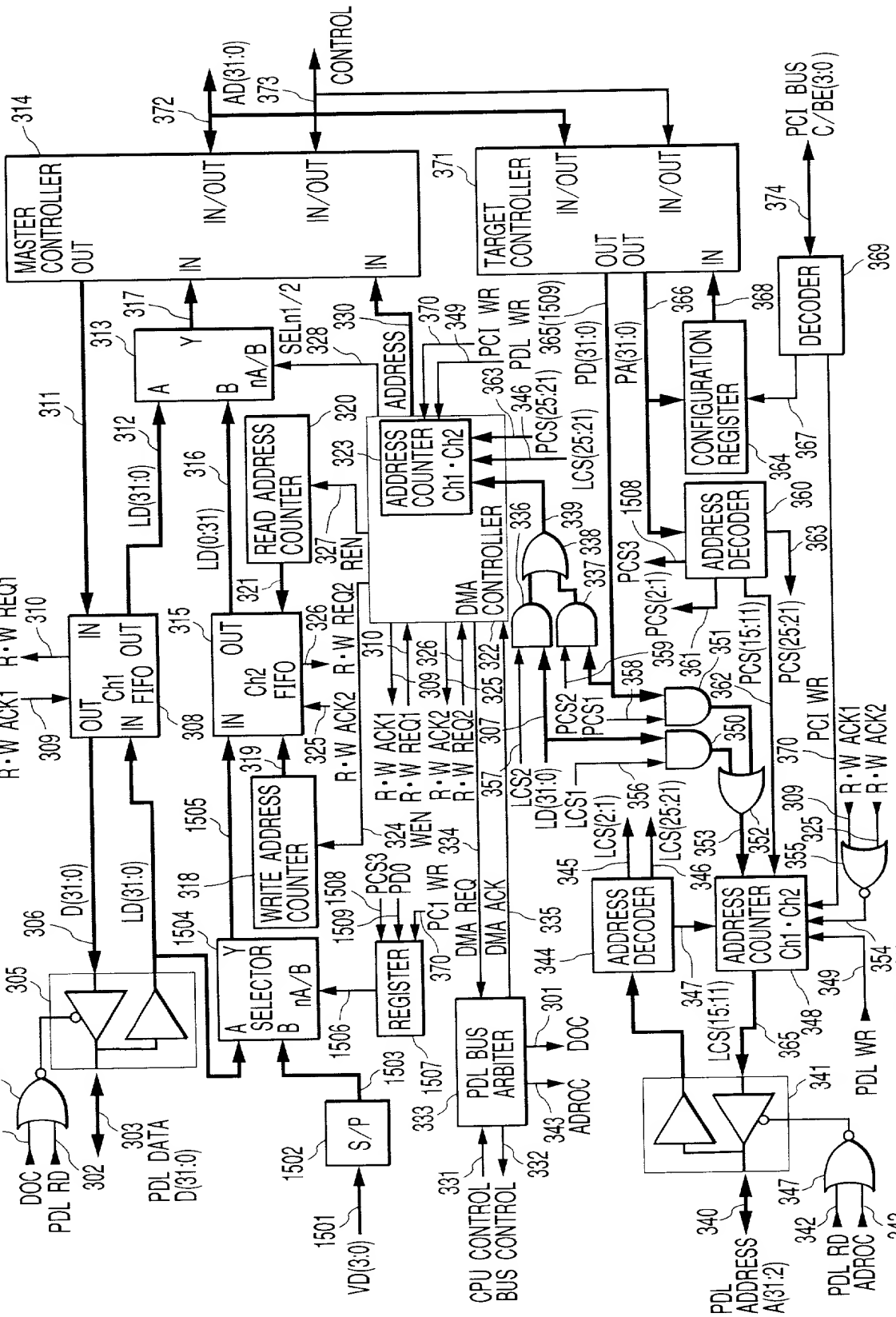
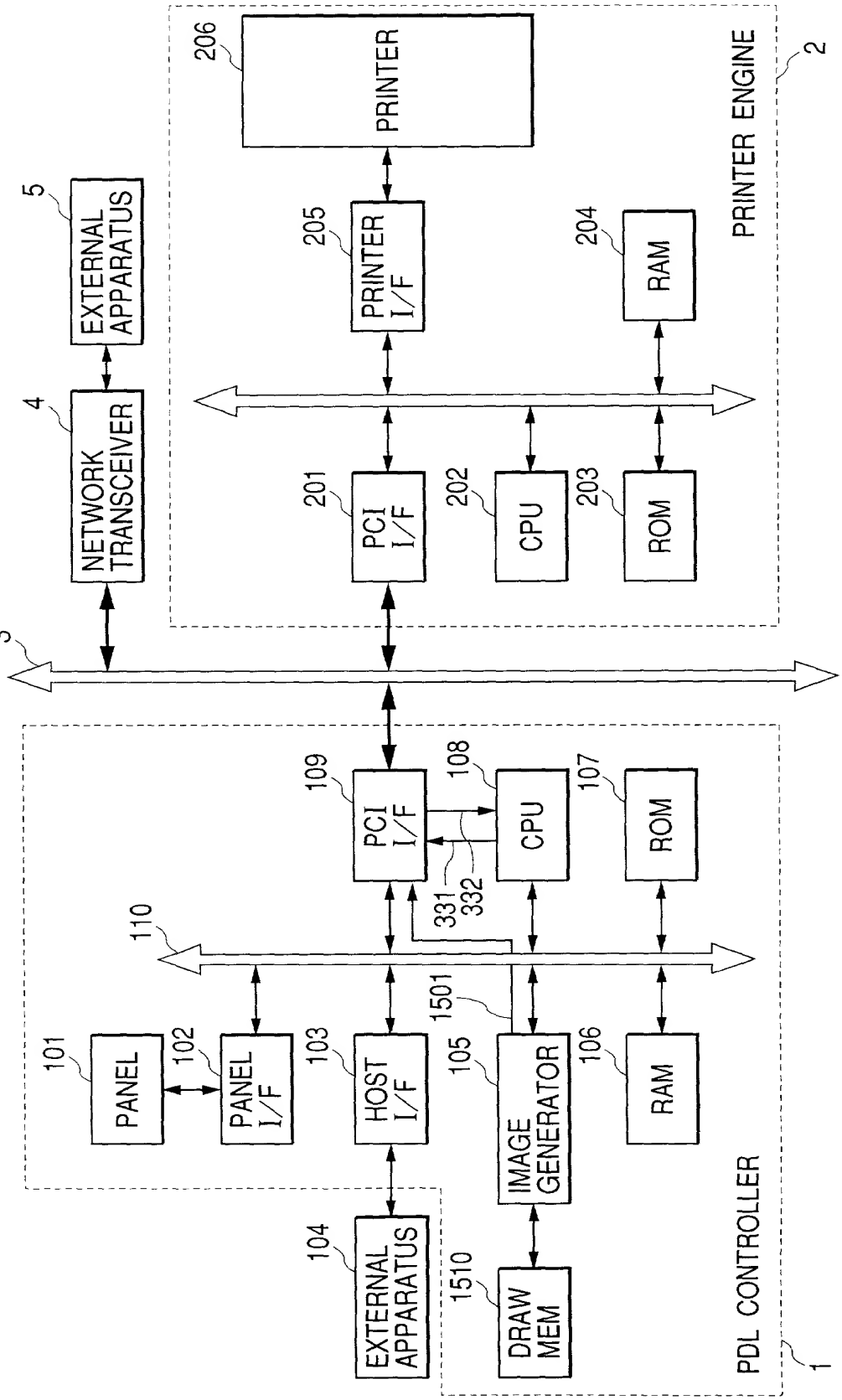

MASTER CONTROLLER
TARGET CONTROLLER
IN/OUT
AD(31:0)
CONTROL
PCI BUS C/BE(3:0)
DECODER
CONFIGURATION REGISTER
ADDRESS DECODER
ADDRESS COUNTER Ch1 · Ch2
READ ADDRESS COUNTER
WRITE ADDRESS COUNTER
Ch1 FIFO
Ch2 FIFO
DMA CONTROLLER
PDL BUS ARBITER
REGISTER
SELECTOR
S/P
R·W REQ1
R·W ACK1
R·W REQ2
R·W ACK2
LD(31:0)
LD(0:31)
D(31:0)
PDL DATA D(31:0)
DOC
PDL RD
PDL WR
R·W ACK
PDL ADDRESS A(31:2)
PDL RD ADROC
CPU CONTROL BUS CONTROL
VD(3:0)
DMA REQ
DMA ACK
PCI WR
PDL WR
ADDRESS
PD(31:0)
PA(31:0)
PCS(25:21)
LCS(25:21)
PCS(15:11)
LCS(15:11)
PCS(2:1)
LCS(2:1)
PCS3
PCS2
PCS1
LCS2
LCS1
LD(31:0)
WEN
REN
PD0
DOC
ADROC

FIG. 25


PDL CONTROLLER
1
PRINTER ENGINE
2
3
4
NETWORK TRANSCEIVER
5
EXTERNAL APPARATUS
101
PANEL
102
PANEL I/F
103
HOST I/F
104
EXTERNAL APPARATUS
105
IMAGE GENERATOR
106
RAM
107
ROM
108
CPU
109
PCI I/F
110
1501
1510
DRAW MEM
201
PCI I/F
202
CPU
203
ROM
204
RAM
205
PRINTER I/F
206
PRINTER
331
332